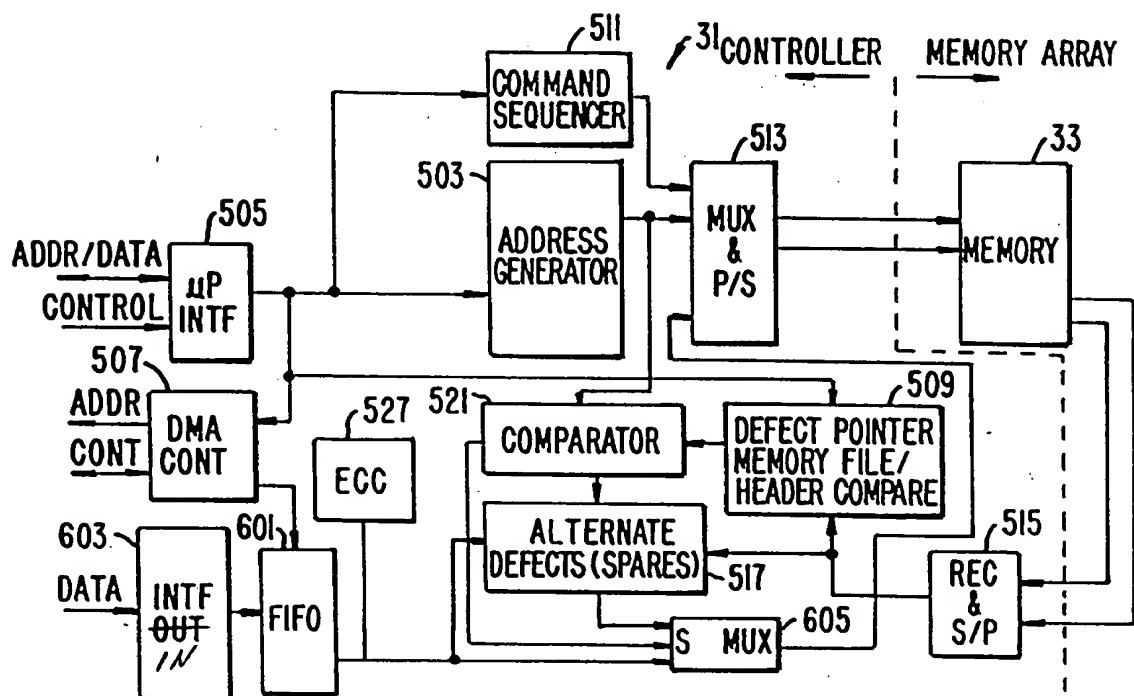


The diagram illustrates a memory system architecture. At the top, a **CONTROLLER** (31) is connected to a **MEMORY ARRAY**. The controller's output goes through a **MUX & P/S** (513) to a **MEMORY** (33). The memory array also feeds back into the controller. A **COMMAND SEQUENCER** (511) is connected to the controller and an **ADDRESS GENERATOR** (503). The address generator outputs to the memory array and also feeds into a **COMPARATOR** (521). A **DEFECT POINTER MEMORY FILE/HEADER COMPARE** (509) is connected to the comparator and the memory array. The comparator outputs to an **ALTERNATE DEFECTS (SPARES)** (517) block. The **ALTERNATE DEFECTS (SPARES)** block outputs to a **MUX** (523). A **DATA** (525) input goes to an **INTF OUT** block, which feeds into a **FIFO** (519). The **FIFO** outputs to the **MUX** (523). The **MUX** (523) outputs to a **REC'D & S/P** (515) block. A **DMA CONT** (507) is connected to the **INTF OUT** block and the **FIFO** (519). An **ECC** (527) block is connected to the **FIFO** (519) and the **COMPARATOR** (521). An **ADDR/DATA CONTROL** (505) is connected to the **INTF OUT** block and the **ADDRESS GENERATOR** (503). A **5/5** label is at the top center.



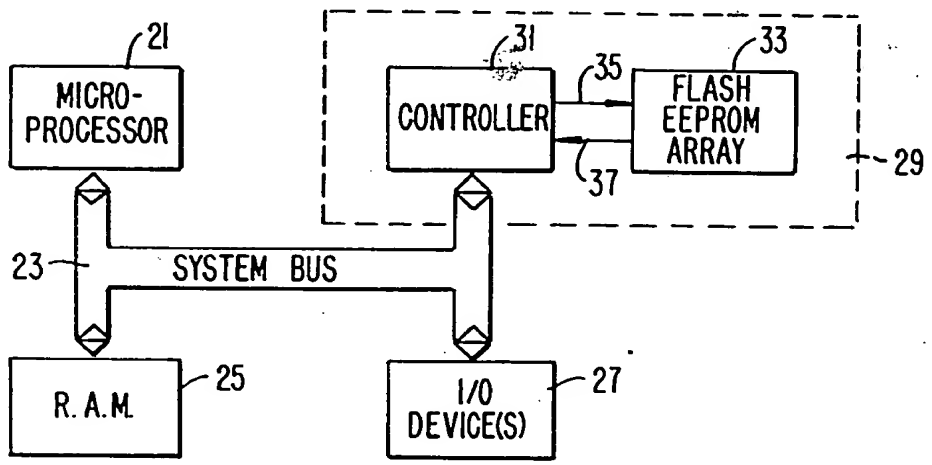


FIG. 1A.

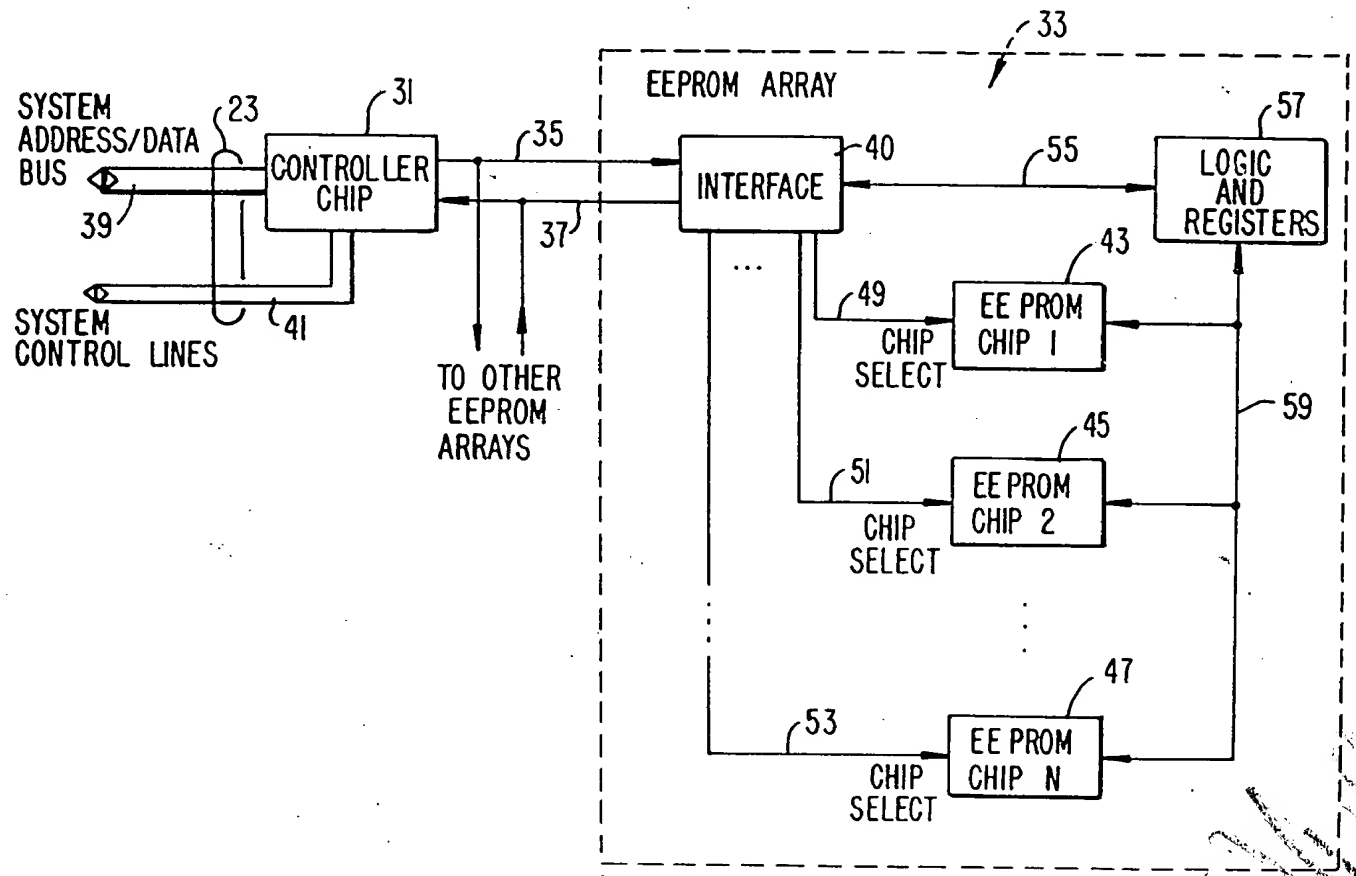


FIG. 1B.

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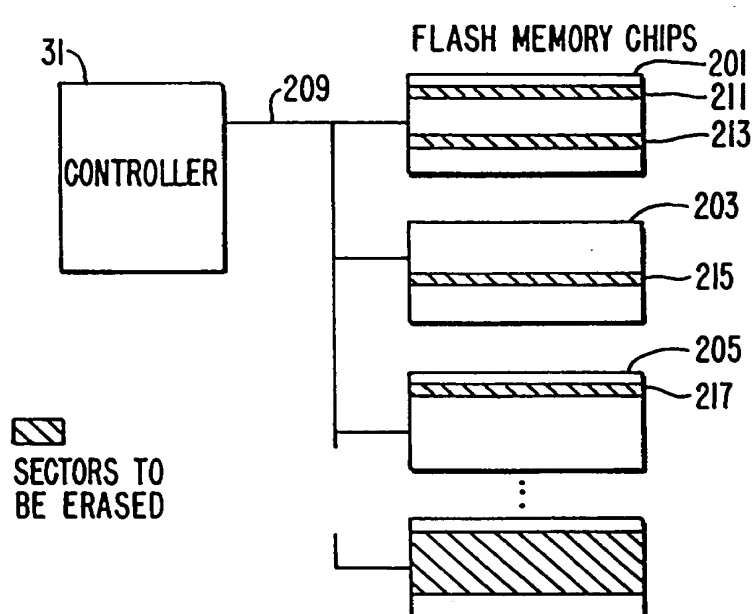


FIG. 2.

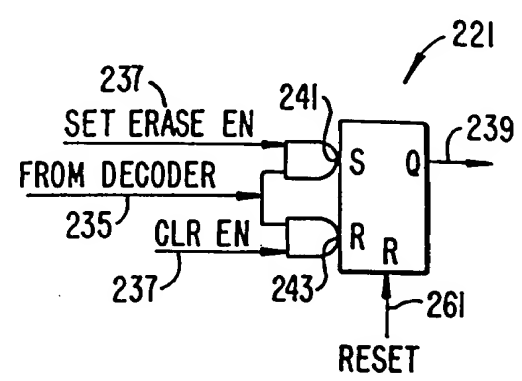


FIG. 3B.

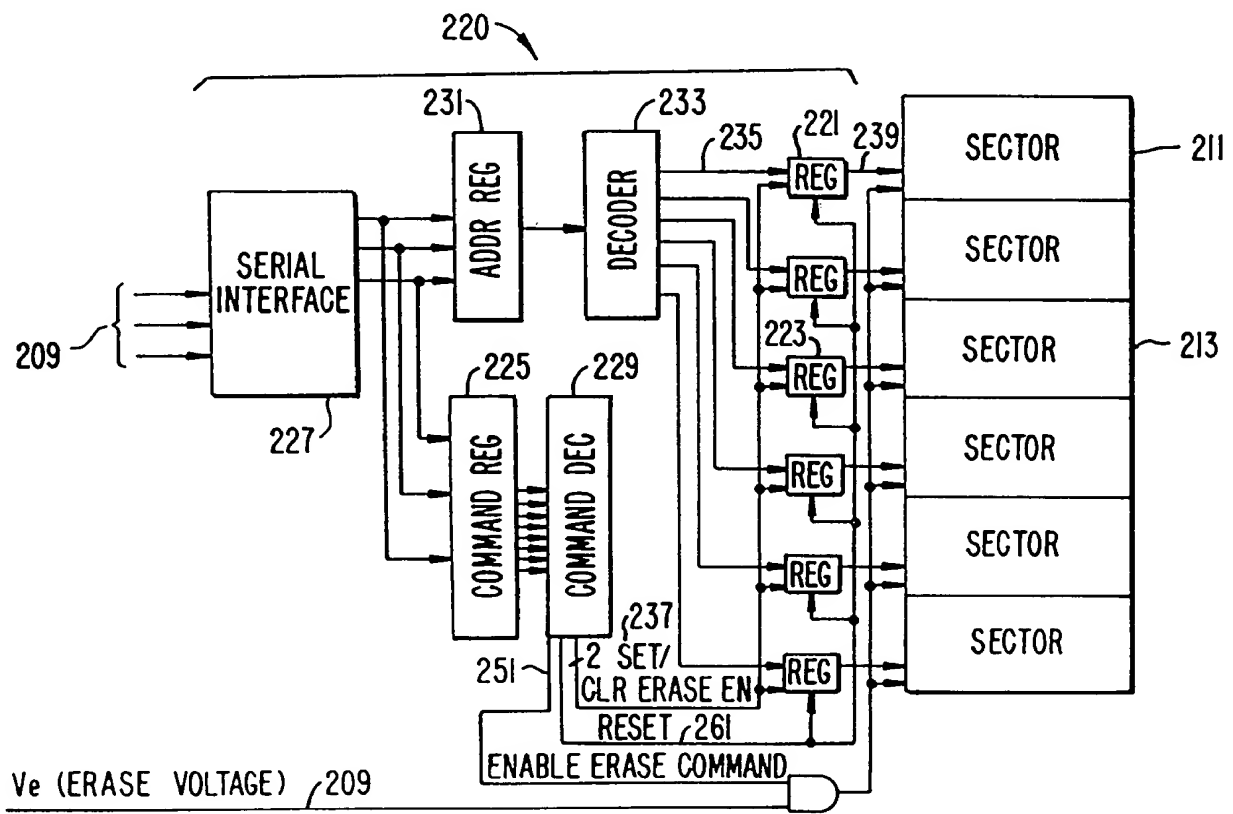


FIG. 3A.

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3/5

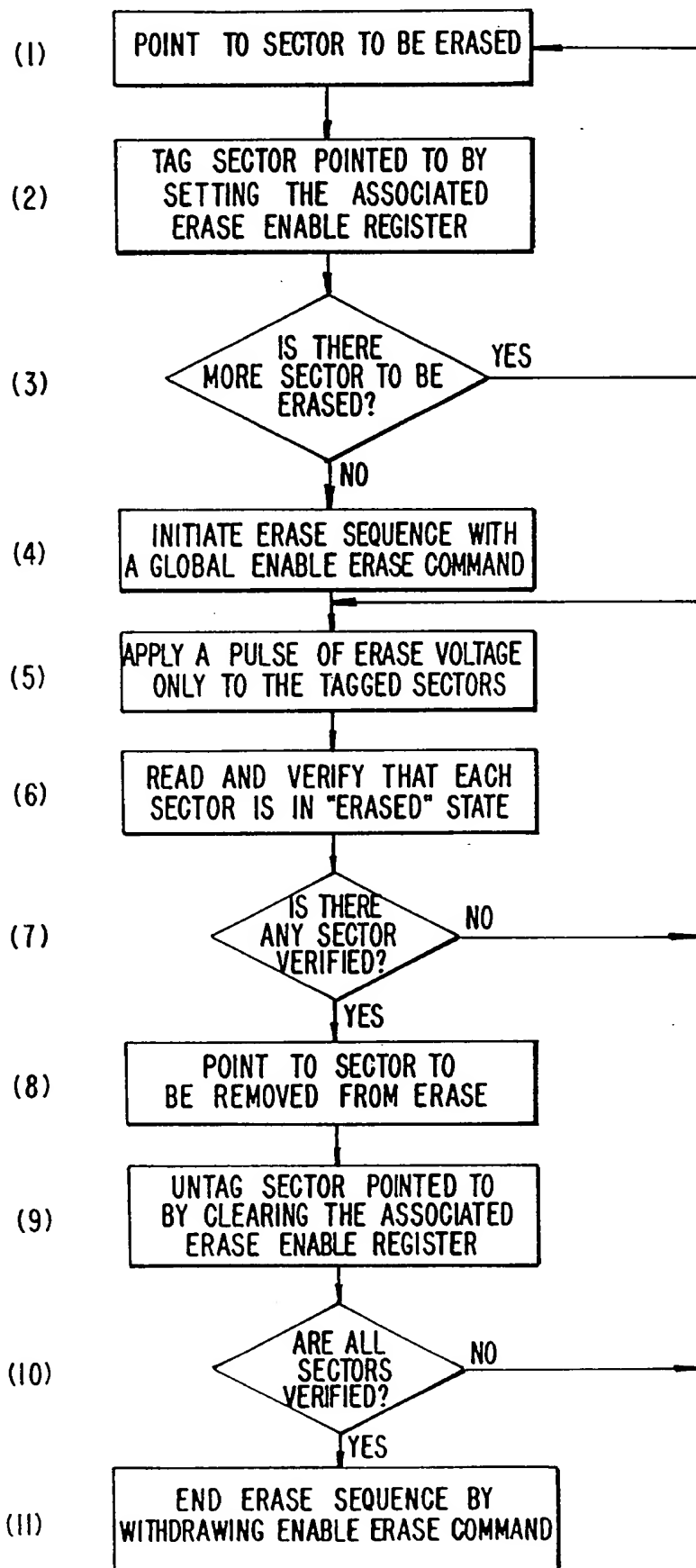
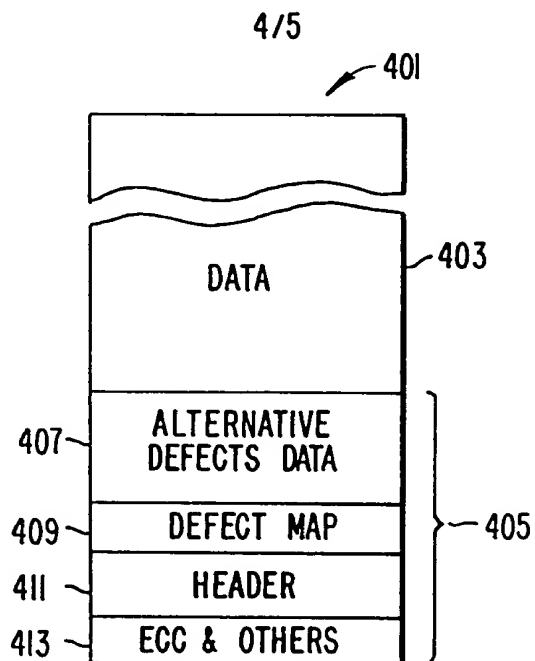


FIG. 4.

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SECTOR PARTITION
FIG. 5.

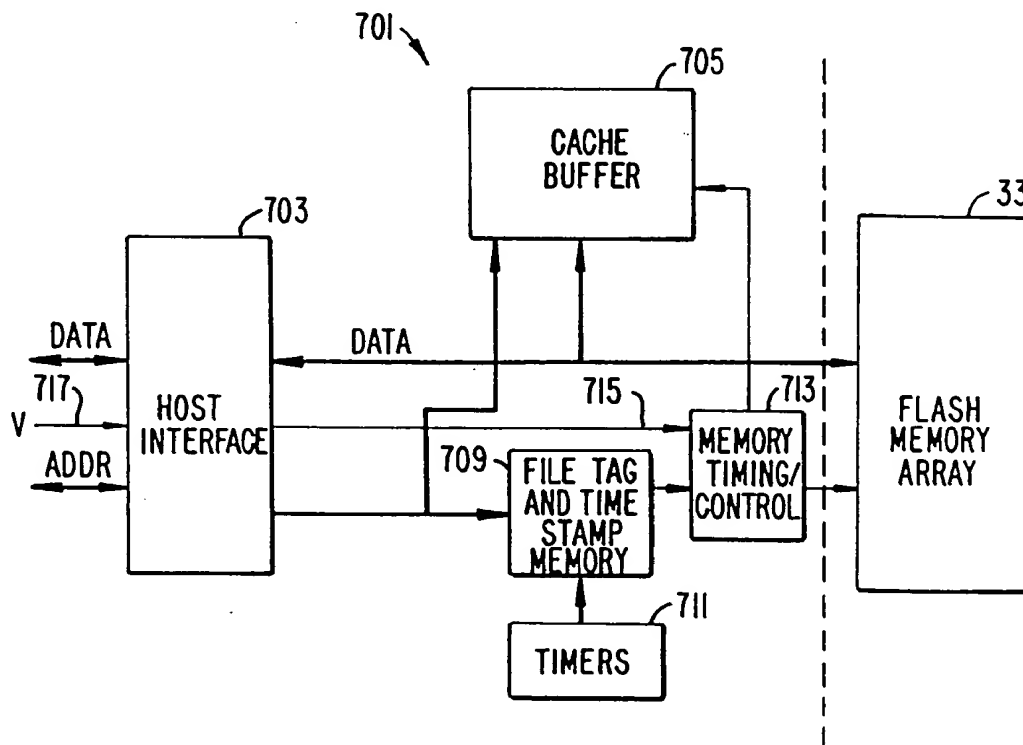


FIG. 8.

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